OSCILLOSCOPE MEASUREMENTS TO SATISFY FULL-BRIDGE CONVERTER VERIFICATION REQUIREMENTS

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CONTENTS

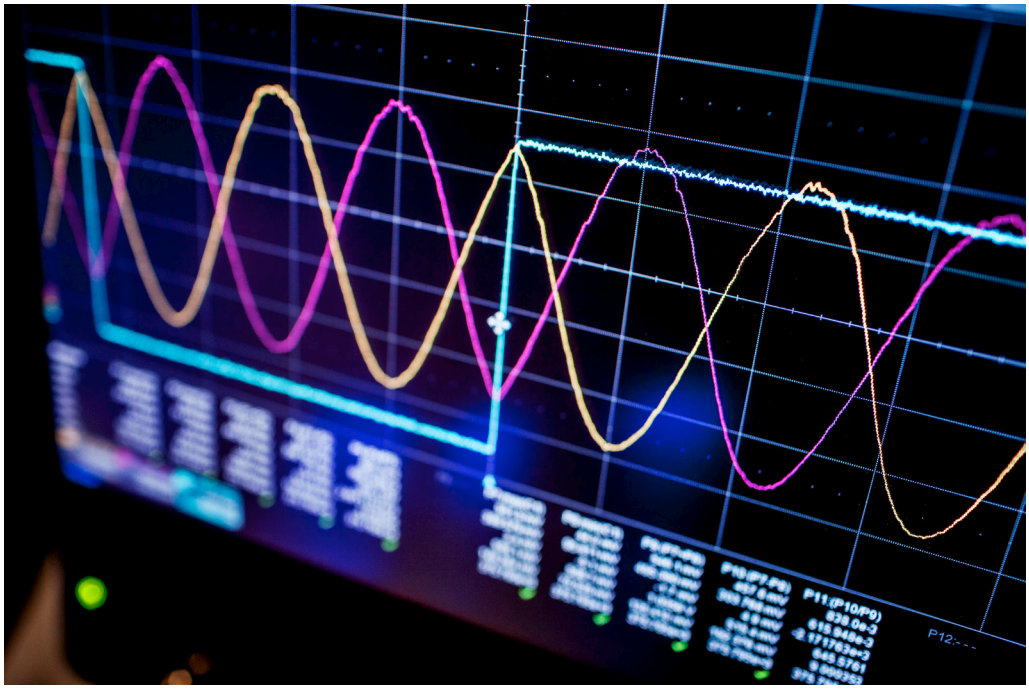
1 INTRODUCTION

Telecommunications and server applications need different types of power architecture to meet current challenges, including a wider range of lower voltage and higher current levels. Distributed power architecture was a common way to deal with these levels, but multiple isolation barriers meant large, expensive bills for components.

Intermediate bus architecture (IBA) has steadily risen in popularity while reducing system sizes and costs, and has increased efficiency and removed the need for multiple isolation barriers. However, testing isolated bus converters (IBC) within this architecture is a complex measurement challenge, since it requires verification of switching patterns in dynamic processes.

Figure 1: Validating full-bridge converters

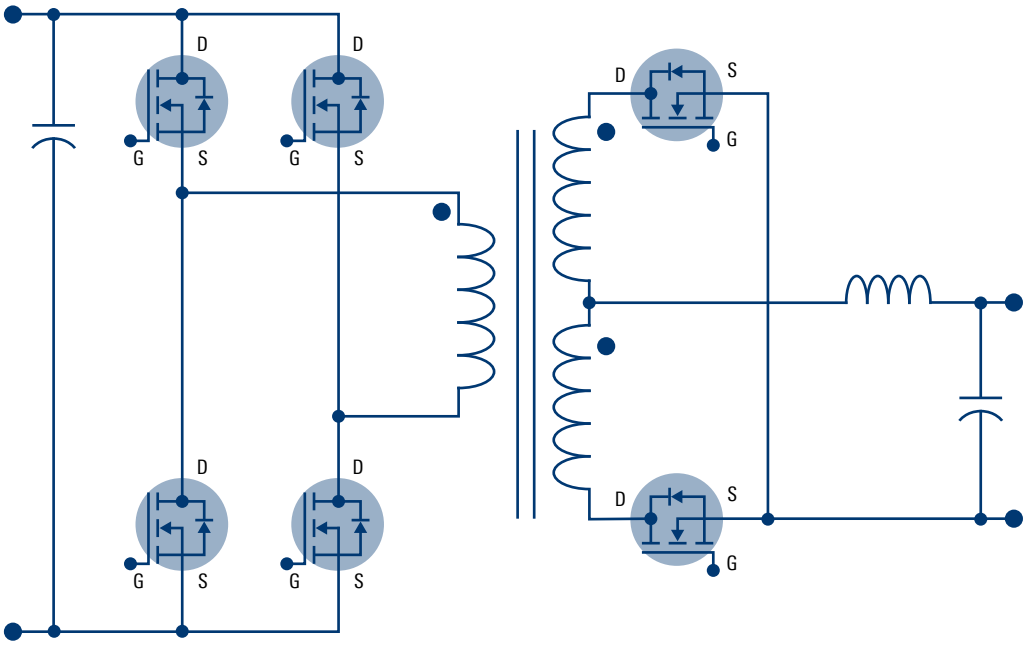
Validating complex circuits such as full-bridge converters requires advanced measurement tools, with a sufficient number of analog channels, memory and functions.



2 WHY THIS METHOD?

The full-bridge converter in Figure 2 has some of the highest efficiency and power output (> 500 W) relative to alternative push-pull (< 200 W) and half-bridge topologies (< 500 W). The increase in power and efficiency makes for excellent transformer utilization but costs more and is more complex since more silicon is integrated into the design. The secondary side uses synchronous rectification to increase efficiency instead of conventional secondary-side rectifying circuits with standard diodes. However, each stage of converter operation must be understood to accurately test this system.

Figure 2: Topology of a full-bridge converter with synchronous rectification



3 THE STAGES OF OPERATION

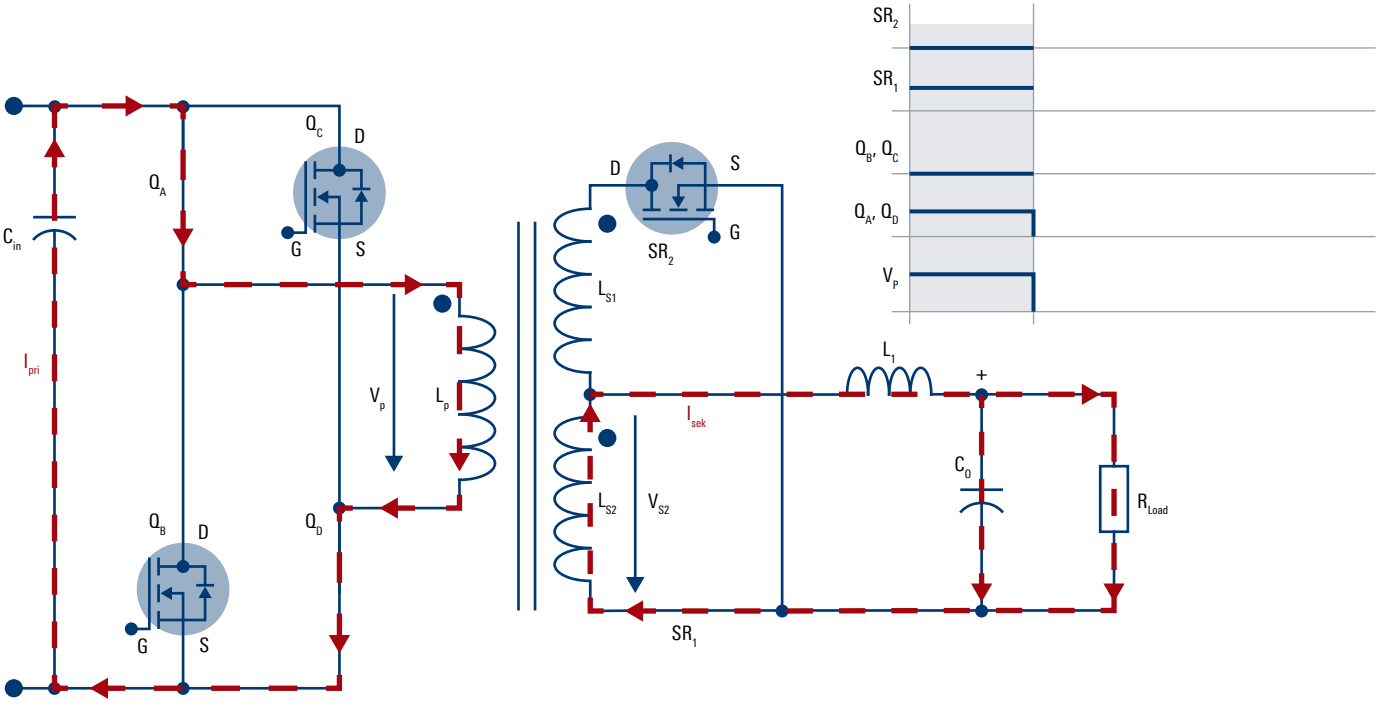
Converter operations can be broken down into four distinct stages.

3.1 Energy transfer cycle I

To begin operation, two diagonally spaced switches (Q_A and Q_D) are switched to the on state to generate a current flow (I_{pri}), energize the primary winding (V_P) and yield an energy transfer to the secondary side (V_{S2}), which creates a current flow in the lower part of the secondary winding (I_{sek}). The current then flows through the power inductor (L_1), through the load (R_{Load}) and the output capacitor (C_O) and back through the winding. During this process, energy is accumulated in L_1 for the next cycle. This stage is captured in Figure 3.

Figure 3: Energy transfer cycle I with corresponding switching pattern

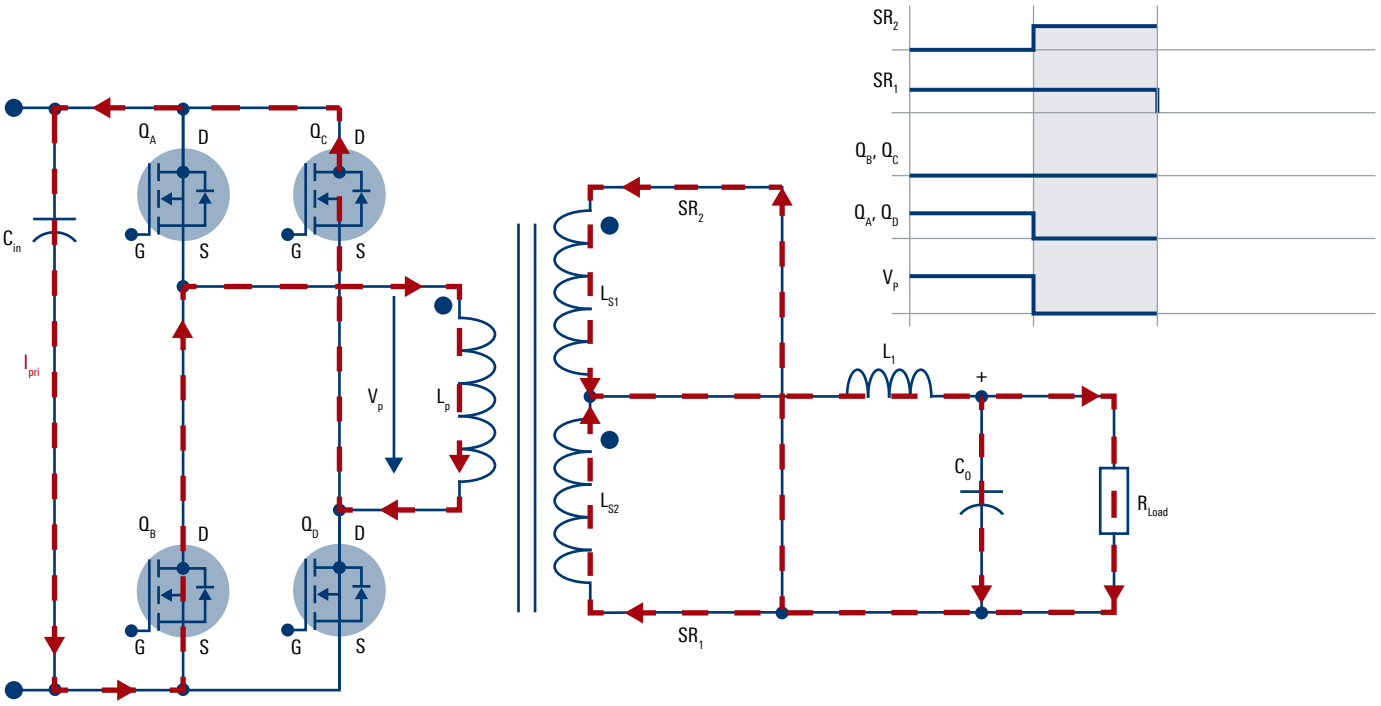
This must be verified at the testing stage.



3.2 Freewheeling cycle I

Figure 4 shows how the next stage opens switches that were previously closed (Q_A and Q_D). However, current flows on the secondary side from the energy stored in the power inductor (L_1) that pushes current into the load (R_{Load}), the output capacitor (C_O) and returns through the secondary windings (L_{S1} and L_{S2}). At this stage both synchronous switches (SR_1 and SR_2) are switched on in a process independent of the primary side. The core leakage inductance (L_P) in the primary winding has energy stored independent of the secondary side and causes current on the primary side to flow uncontrollably through the Q_C and Q_B body diodes.

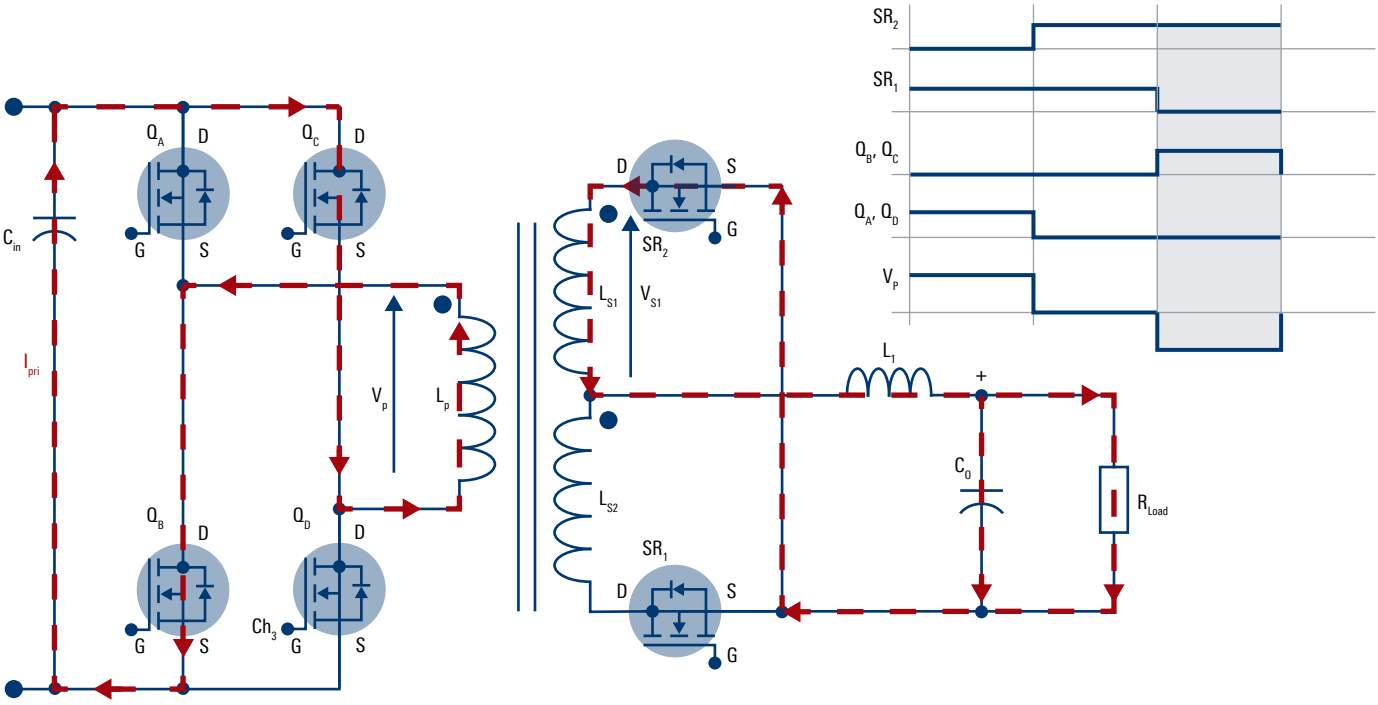
Figure 4: Freewheeling cycle I with corresponding switching pattern in gray



3.3 Energy transfer cycle II

Figure 5 shows how energy transfer cycle II switches on the other two diagonally-spaced switches (Q_B and Q_C) cause current flows in the direction opposite to freewheeling cycle I, energizing the primary winding (L_P) and transferring energy to the secondary side (L_{S1}) with a secondary current flow (I_{sek}). The synchronous rectifier switch (SR_2) is turned on at the same time to reduce conduction losses. Once again, energy is accumulated in the L_1 power inductor and pushing current into R_{Load}.

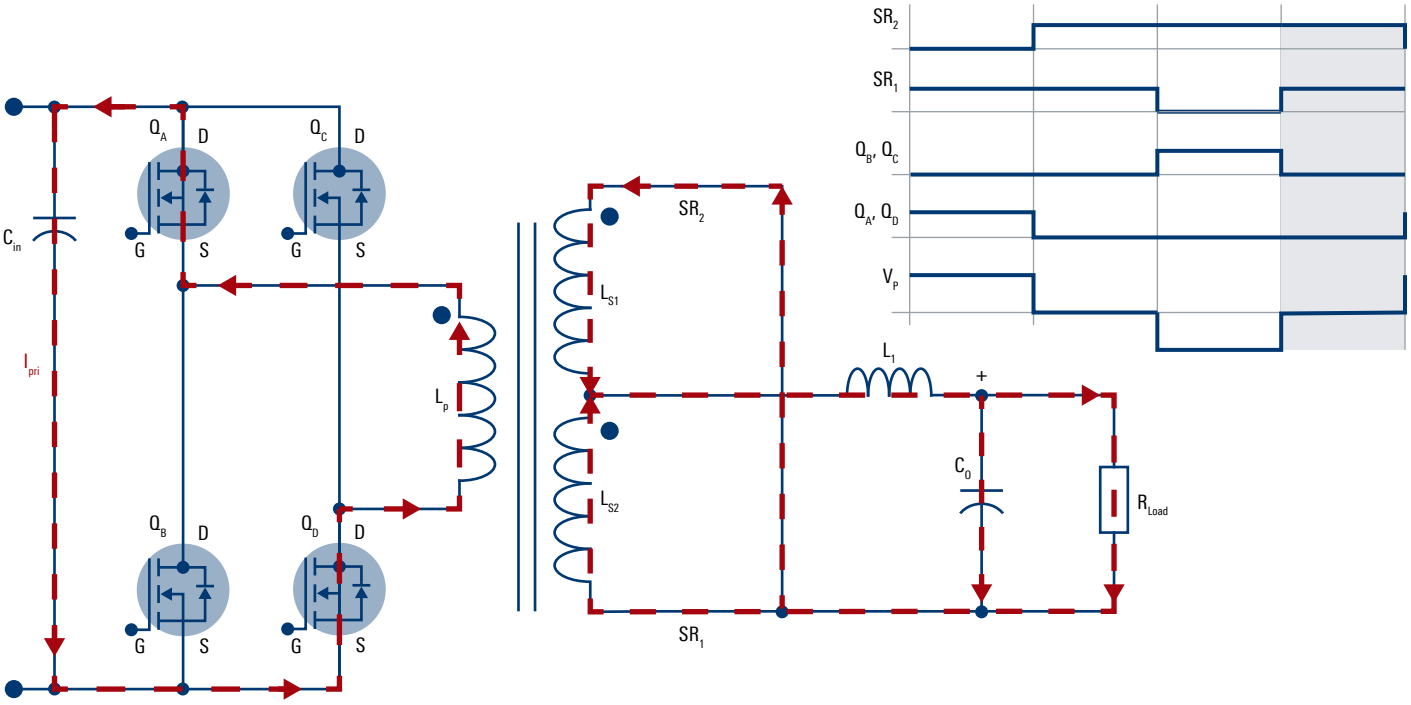
Figure 5: Energy transfer cycle II



3.4 Freewheeling cycle II

Finally, another freewheeling cycle concludes the switching pattern: current independently flows on the secondary side thanks to the energy accumulated in L_1 (Figure 6). The leakage inductance L_P also causes a current flow on the primary side. It is important to verify operation of the digital controller to ensure the switches are operated so the switching states correlate correctly.

Figure 6: Freewheeling cycle II stage where the current induced through L_1 creates a flow through the secondary side, turning on SR_1 and SR_2



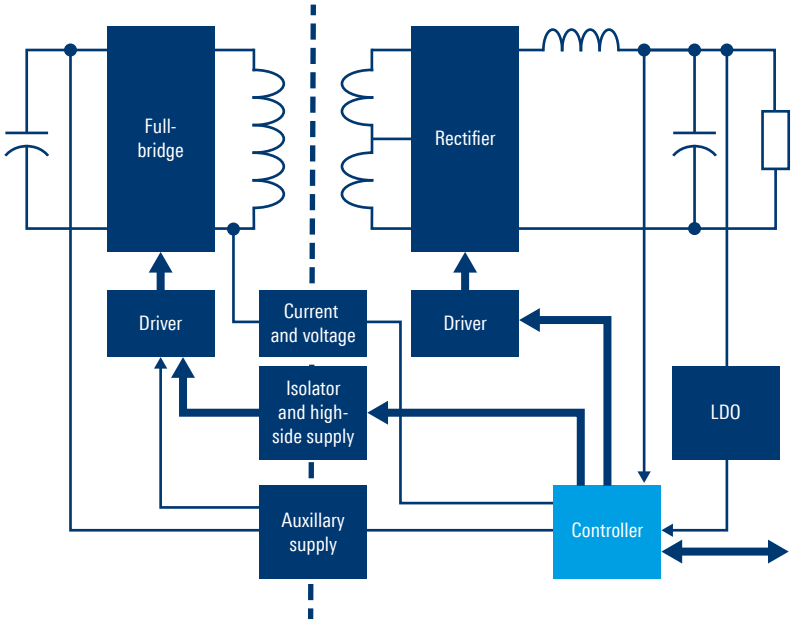
4 FULLY ISOLATED SYSTEM DESIGN

Figure 7 shows a fully fleshed out isolated system beyond the power stage. The additional components include a controller to transfer and receive information from the circuit. On the secondary side, no isolation barrier drives the rectifier and the switches require information through the isolation barrier with isolators to drive the full-bridge converter. Note that the isolators introduce a delay from the controller to the full-bridge that must be measured and included in dead-time calculations.

At start-up, the secondary side of the circuit has no potential to supply the controller. The auxiliary supply provides energy to the controller at start-up and brings the converter to a steady-state to supply the controller. Testing the start-up phase with an auxiliary supply can be very complex.

Figure 7: Isolated system

The full-bridge converter on primary side and rectifier on secondary side with a controller and associated circuits that must perform their functions while providing an isolation barrier



5 VERIFYING CONVERTER SWITCHING PATTERN WITH THE MXO 5

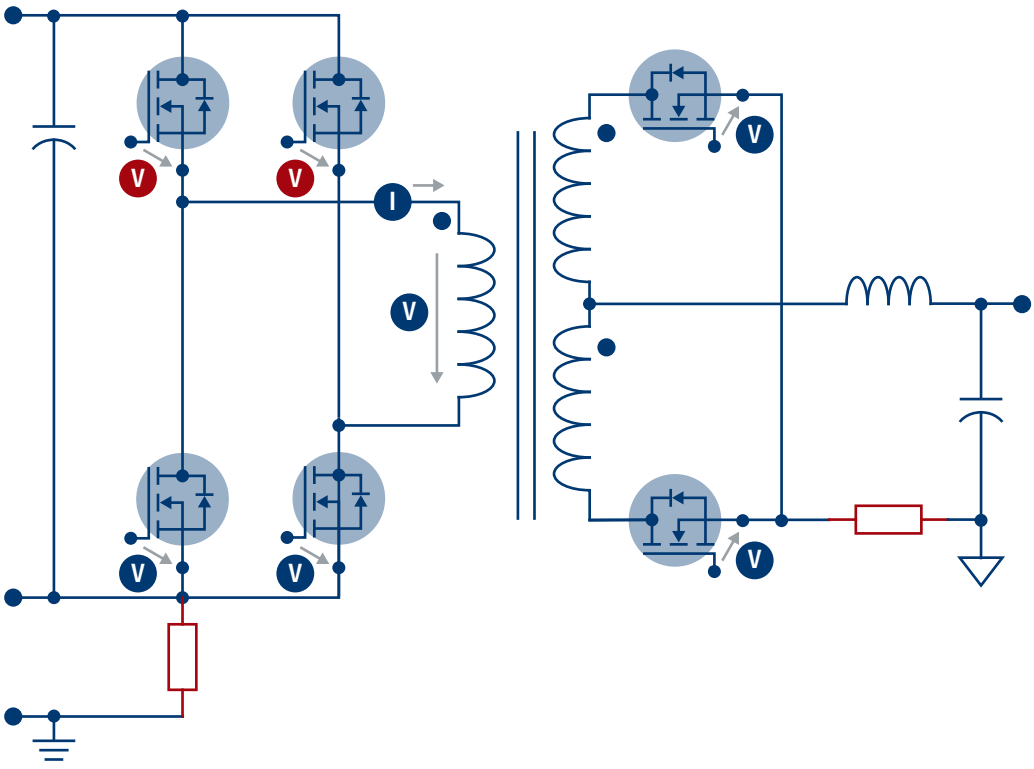
5.1 Necessary probe points

A conventional four-channel oscilloscope could not test the fully isolated system. To validate all switching states and their correlations, at least six channels are required for the following:

- The gate-source voltage for the two low-side switches
- The gate-source voltage for the two synchronous rectifiers
- The voltage across the primary winding
- The current across the primary winding

These primary probe points (blue V and I) are shown in Figure 8. Another two potential probing points for gate-source voltage in the two high-side switches (red V) ensure the diagonally spaced switches can operate simultaneously.

Figure 8: Necessary probe points in the isolation system to verify switching patterns



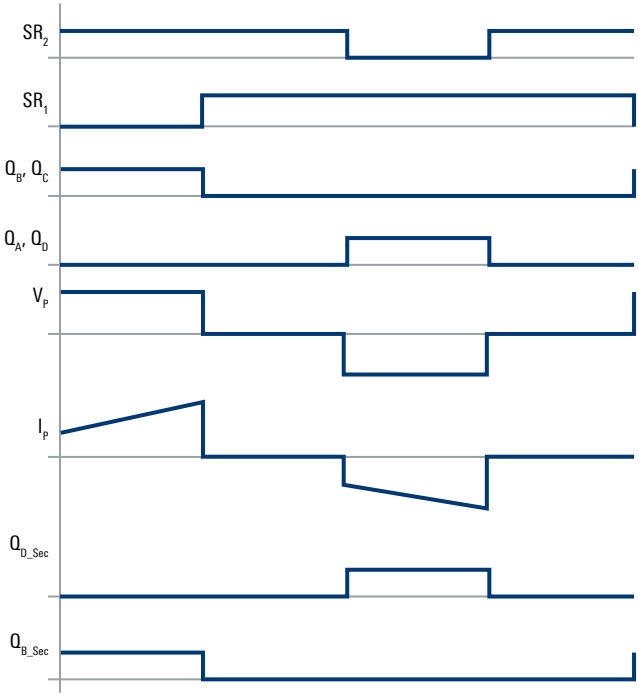
5.2 Differential probes

Another major requirement is for differential probes. The shunts that measure current on the primary (red in Figure 8) and secondary will violate the isolation barrier when connecting passive probes with grounds. If the passive probes are grounded at the shunt, they would short the current measurement system. Shorting the two different grounds together also needs to be prevented.

5.3 Switching pattern requiring verification

The probe points verify the ideal switching patterns in Figure 9. Three additional waveforms are not included in the basic switching patterns in Figures 3 through 6 (I_P, Q_{D_Sec}, and Q_{B_Sec}). The I_P waveform monitors and analyzes the transformer to ensure the core is not saturated. The Q_{D_Sec}, and Q_{B_Sec} waveforms are measured on the secondary side, directly at the controller. This necessary waveform measures the delay between the primary and secondary switches (isolator). The delay is measured between Q_D and Q_A with Q_{D_Sec} and between Q_B and Q_C with Q_{B_Sec}. Once this setup is activated, users can easily identify oscillations, overshoots, undershoots and the rise and fall times to gather as much useful information as possible and characterize the device under test (DUT).

Figure 9: The switching pattern that must be verified at the testing stage



5.4 Switching pattern results

The results of the probing pattern in Figure 9 is shown in Figure 10. The channels are as follows:

- Channel 1 (TrDiff): voltage of primary winding
- Channel 2 (TrCurr): current of primary winding
- Math channel (M1): Channel 2's current information converted and displayed in amps
- Channel 3 (SR2): gate-source voltage of the synchronous rectifier SR_2
- Channel 4 (SR1): gate-source voltage of the synchronous rectifier SR_1
- Channel 5 (GateD): gate-source voltage of the low-side switch Q_D
- Channel 6 (GateB): gate-source voltage of the low-side switch Q_B
- Channel 7 (Q_{D_Sec}): Q_D and Q_A switches measured on the secondary side, at the controller
- Channel 8 (Q_{B_Sec}): Q_B and Q_C switches measured on the secondary side, at the controller

The cycles are readily visible within the top window including the voltage and current measurements on the primary winding. A table shows the delay between the synchronous rectifier switches and the primary switches as well as the delay between the primary and secondary switches (isolator). All relevant information is readily available, letting users make quick assessments and repeat tests at different working points (e.g. input voltage levels, output current levels) where switching patterns might need to be confirmed, including all delays and oscillations, and that these are correct and within specifications.

Figure 10: Screenshot of oscilloscope including all information to validate the converter switching pattern

6 VALIDATING START-UP SEQUENCES WITH THE MXO 5

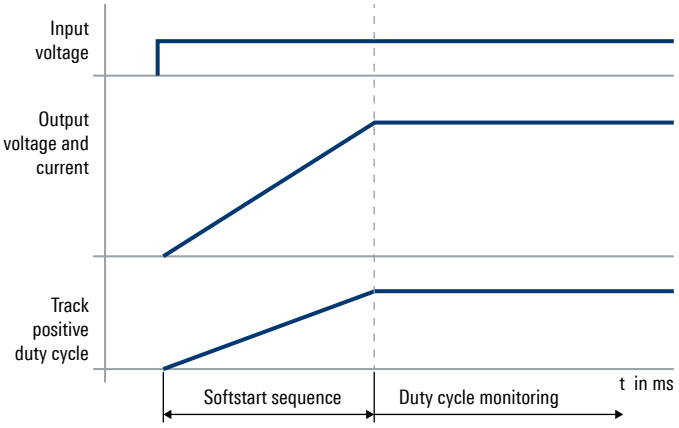
6.1 Necessary probe points

Converter testing also involves validating start-up sequences with an auxiliary power supply. This testing is generally one of the most complex measurements for any converter since the start-up sequence is a dynamic process that involves many signals and small issues can prevent the system from running properly. The required probes are identical to the previous example, with output voltage and current added to determine if a system has reached a steady state.

6.2 Start-up aspects needing verification

Figure 11 shows typical input voltage, output voltage and current waveforms. The input voltage at the start yields an output voltage and current that increases gradually in a specified amount of time to avoid current overshoots or fast edges. Eventually this softstart brings the converter to a steady state. This test instrument must have a long acquisition period at a high sample rate to visualize everything properly, which requires a high amount of memory.

Figure 11: The oscilloscope used must be able to support a long acquisition with a high sample rate to analyze the sequence using proper tools



6.3 Start-up measurement results

The results of the start-up measurement can be seen in Figure 12. The probe points for channels 1 to 6 are identical to the previous section.

- Channel 7: output voltage (V_{out})
- Channel 8: output current (I_{out})

The top window shows voltage and current on the primary winding. In the bottom window, the output voltage (channel 7: V_{out}) is easily identifiable with a slow, increasing slope until the converter reaches a steady state. There is also a noticeable spike in current (inrush current) as shown in the dark purple waveform (channel 8: Iout) that can be optimized for constant current. However, insight is now limited due to the difficulty of zooming into functions with long acquisitions, better to measure the duty cycle on a cycle-by-cycle basis and define a track function that shows the duty cycle variation over time.

Figure 12: Start-up verification results showing a spike in current

These standard settings can limit insight into the waveforms.

6.4 Start-up results with track function

Figure 13 shows the start-up results where a display for pulse width modulation (PWM) information tracks waveforms. Two track functions include the primary switches and synchronous rectifiers, each of which behave differently. The primary switches go from a low-duty cycle to steady state, while the synchronous rectifiers begin rapidly and then slightly decrease in the duty cycle, before entering a steady state. Note that the synchronous rectifiers are not critical at start-up and may be unnecessary to switch on until the system has reached a steady state. Further investigation reveals that the undesirable current spike in Figure 12 is from a sharp increase in the duty cycle of the synchronous rectifiers during start up.

Also note the blue waveform (channel 4: SR2_Digital) seen in the same window as the track function for the synchronous rectifier: this is digital information directly probed at the controller. It was the source of the track function, since it requires a stable amplitude. This contradicts the alternative analog orange waveform that measures the gate-source voltage for the synchronous rectifier SR_2 (channel 3: SR2), where amplitude changes as the output voltage ramps up. As a rule of thumb it is better to use pure digital circuits since they have constant amplitudes.

Figure 13: Using the track function with the synchronous rectifiers and primary switches reveals a sharp increase in duty cycle upon start-up

7 CONCLUSION

Validating complex circuits such as full-bridge converters requires advanced measurement tools, with a sufficient number of analog channels, memory and functions.

The MXO 5 from Rohde&Schwarz has eight analog channels for robust testing of full-bridge converters, where all the relevant waveforms can be viewed on a single screen. This is directly relevant to converter verification and especially the validation of the start-up process.

Contact the experts at Rohde&Schwarz to learn more about the MXO 5:
www.rohde-schwarz.com/contact_63733.html

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Oscilloscope measurements to satisfy full-bridge converter verification requirements
Data without tolerance limits is not binding | Subject to change